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A Unified Approach to Resilient Zonal E/E Architectures: TSN-Aware Communication, Lockstep Fault Tolerance, and Secure OTA Management

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ABSTRACT

This article presents a comprehensive, original synthesis and theoretical expansion of contemporary developments in automotive electrical/electronic (E/E) architectures, with a special focus on zonal topologies, time-sensitive networking (TSN), service-oriented architectures (SOA), and fault-tolerant lockstep processors for safety-critical controllers. The work builds strictly on the references provided, integrating evidence from industry technical papers, conference proceedings, and journal articles to propose an extended conceptual framework that reconciles real-time determinism, cybersecurity, and functional safety within evolving centralized-to-zonal migration strategies. Methodologically, the paper undertakes a structured conceptual analysis that triangulates (1) TSN configuration and management techniques (Chahed & Kassler, 2021; Hackel et al., 2022), (2) SOA/OPC UA integration with AUTOSAR Adaptive (Arestova et al., 2021; Villanueva et al., 2021), (3) drivetrain and advanced driver assistance system (ADAS) control under network-induced delays (Cao et al., 2019; 2021; 2022; 2023), and (4) hardware redundancy strategies exemplified by dual-core lockstep designs (Abdul Salam Abdul Karim, 2023). The Results section elaborates an enriched architecture blueprint that balances QoS predictability, deterministic latency, and modular service interfaces, and delineates tradeoffs among centralization, zonalization, and gateway optimization (Bandur et al., 2021; Sander et al., 2011). In Discussion we examine theoretical implications, limitations, and propose a prioritized research and validation agenda to move from conceptual design toward industrial validation. The Conclusion summarizes the principal contributions and enumerates concrete next steps for researchers and practitioners seeking to implement resilient, TSN-aware zonal E/E systems for next-generation autonomous and electrified vehicles

Keywords

Zonal E/E architectures; time-sensitive networking; service-oriented architecture; fault-tolerant lockstep; hardware–software co-design

1. Introduction

The automotive industry is undergoing a structural transformation in electrical/electronic (E/E) architecture design driven by rising software content, electric powertrain integration, and advanced driver assistance and automated driving functions. Historically, distributed ECUs connected by CAN and LIN buses served a component-centric model. Contemporary trends push toward zonal, domain-centralized, or even vehicle centralized E/E topologies to improve maintainability, reduce wiring complexity, and enable high-bandwidth sensor and compute consolidation (Bandur et al., 2021; Frigerio et al., 2021). Simultaneously, deterministic, low-jitter communications and service abstractions—enabled by Time-Sensitive Networking (TSN) and Service-Oriented Architectures (SOA)—are

emerging as pivotal enablers for predictable, real-time inter-ECU exchanges that must coexist with legacy buses and strict functional safety requirements (Chahed & Kassler, 2021; Arestova et al., 2021; Villanueva et al., 2021).

This article addresses the central problem of reconciling three often competing objectives in modern vehicle E/E architecture design: (1) real-time determinism for safety-critical control loops, (2) flexibility and scalability for software-defined services (e.g., OTA updates, diagnostics, cloud interfacing), and (3) cost- and energy-efficient hardware design suitable for mass production. Prevailing literature documents these components—TSN enabling deterministic Ethernet (Brunner et al., 2017; Chahed & Kassler, 2021), SOA integration paths for AUTOSAR Adaptive via OPC UA (Arestova et al., 2021), and fault-tolerant dual-core lockstep hardware for zonal controllers (Abdul Salam Abdul Karim, 2023)—but lacks a fully integrated blueprint that explicates the hardware–software co-design rules, QoS provisioning strategies, gateway synthesis, and safety/cybersecurity interplay necessary for industrial deployment. Moreover, control system analyses have documented the sensitivity of advanced control functions (adaptive cruise control, drivetrain, AEB) to network-induced delays and heterogenous loop latencies (Cao et al., 2019; 2021; 2022; 2023), but a comprehensive mapping from network QoS profiles to controller design constraints in zonal TSN ecosystems remains underdeveloped.

This work fills that gap by synthesizing insights from the referenced corpus and substantially extending them through theoretical elaboration. We articulate a modular, layered architecture where TSN switches and schedulers provide deterministic scaffolding, SOA/OPC UA provides service abstraction and discoverability, and zonal hardware nodes adopt lockstep or selective redundancy strategies based on ASIL-driven function criticality. Our objective is not merely to repackage existing proposals, but to distill precise design rules, tradeoff curves, and verification pathways that can guide engineers in mapping system-level safety and performance targets to concrete TSN configurations, SOA partitioning strategies, and hardware redundancy choices.

Methodology

Because the user supplied a bounded set of references, this research uses a rigorous conceptual synthesis method rooted in cross-reference analysis and theoretical model building. The method involves four interleaved analytical activities conducted iteratively: (1) thematic extraction and mapping, (2) systems-level constraint articulation, (3) co-design rule derivation, and (4) hypothetical validation through use-case mapping. Each step is described below.

Thematic extraction and mapping: Each provided reference was reviewed to extract its central claims, architectures, experimental results, and normative recommendations. For TSN and SDN management aspects, Chahed & Kassler (2021) and Hackel et al. (2022) supplied configuration paradigms and security constraints; these were mapped onto TSN feature sets (time-aware shapers, credit-based shapers, frame preemption) and control plane strategies. For SOA and AUTOSAR Adaptive integration the OPC UA proposals from Arestova et al. (2021) and Villanueva et al. (2021) were analyzed to identify service discovery, abstraction, and QoS mapping mechanisms. For control systems, Cao and colleagues' multiple studies (2019; 2021; 2022; 2023) provided models of how variably compounded network delays and hetero-integration loops impair stability and performance; these were used to derive latency budgets and jitter sensitivity thresholds for representative control loops. Hardware redundancy and zonalization literature (Abdul Salam Abdul Karim, 2023; Bandur et al., 2021; Buttle & Gold, 2022; Schäfer & Denkelmann, 2018) informed the classification of controllers and the mapping of ASIL levels to redundancy schemes.

Systems-level constraint articulation: From the thematic maps we articulated explicit constraint families that any candidate architecture must satisfy: deterministic end-to-end latency (control loop deadlines), fail-operational/fail-safe thresholds (safety), QoS isolation (non-interference among service classes), gateway latency bounds (legacy bus integration), bandwidth provisioning (sensor fusion needs), and cybersecurity attack surface minimization (secure control plane and data plane). Each constraint family was parameterized where possible using values and

ranges referenced in the source works (e.g., control deadlines reported in automotive control literature; TSN-related latency and jitter characteristics discussed by Chahed & Kassler, 2021).

Co-design rule derivation: We synthesized rule sets that map system requirements to design choices. Rules include: how to select TSN scheduling classes for different service types, when to select lockstep dual-core processors versus single-core with watchdogs, how to dimension zonal switch fabric and gateway throughput, and how to allocate functions between centralized and zonal units according to latency and redundancy needs (Bandur et al., 2021; Abdul Salam Abdul Karim, 2023). Each rule was justified with reference to the literature and expanded with theoretical implications and counter-arguments.

Hypothetical validation through use-case mapping: To ground the derived rules, three representative use cases were modeled conceptually: a) high-speed lane-keeping steering intervention (stringent deadline, high safety requirement); b) coordinated adaptive cruise control (penetrative of network delays per Cao et al., 2021); and c) infotainment and telematics (high bandwidth, low criticality). For each use case, we traced the mapping of function → service class → TSN configuration → hardware redundancy selection, and we described verification metrics and test sequences (processing latencies, packet loss tolerance, failover timelines).

Throughout, all major claims were linked to the supplied references using the (Author, Year) citation format. Where empirical numerical ranges were not in the references, we explicitly flagged assumptions and derived qualitative tradeoffs instead of inventing unsupported numeric claims.

Results

The output of the conceptual synthesis is a detailed, integrated architecture blueprint and an accompanying set of prescriptive co-design rules. The Results section describes: (1) the layered architecture model, (2) QoS and TSN provisioning framework, (3) function classification and hardware redundancy mapping, (4) gateway and legacy integration approach, and (5) verification and validation roadmap. Each subsection is elaborated at length to provide concrete guidance.

Layered architecture model: We propose a four-layered conceptual architecture: Physical & Zonal Layer, Deterministic Network Layer (TSN fabric), Service Abstraction Layer (SOA/OPC UA + AUTOSAR Adaptive runtimes), and System Management Layer (SDN/management, cybersecurity, OTA). The Physical & Zonal Layer consolidates sensors, actuators, and powertrain controllers into geographically adjacent hardware zones to reduce wiring length and concentrate I/O (Bandur et al., 2021; Schäfer & Denkelmann, 2018). Within a zone, a zonal controller—potentially implemented on an SoC family such as NXP S32G or equivalent—is the primary compute endpoint for local control loops. The Deterministic Network Layer comprises an in-vehicle TSN fabric with time-aware shapers (TAS) and preemption enabled to enforce hard scheduling for high-priority control frames while concurrently carrying lower-priority service traffic (Brunner et al., 2017; Chahed & Kassler, 2021). The Service Abstraction Layer uses OPC UA and AUTOSAR Adaptive patterns to publish and subscribe to services with explicit QoS metadata, enabling discovery and loose coupling while retaining deterministic pathways for critical data (Arestova et al., 2021; Villanueva et al., 2021). The System Management Layer implements a software-defined control plane for TSN configuration, dynamic reconfiguration, and security policy enforcement, drawing on SDN paradigms (Chahed & Kassler, 2021; Hackel et al., 2022).

QoS and TSN provisioning framework: The TSN fabric must provide service classes mapped to function criticality and control loop deadlines. We define three principal classes:

• Control-Deterministic Class (CDC): For real-time, safety-critical control loops (e.g., lateral control actuators, emergency braking). CDC uses TAS with tightly bounded schedule windows, explicit time synchronization (gPTP), and minimal queuing. The prescriptive rule is to provision TAS windows such that worst-case end-to-end latency

budget for control frames is less than the most conservative stability margin derived from control system sensitivity (Cao et al., 2019; 2021; 2022).

• Coordinated Safety Class (CSC): For multi-ECU coordinated functions like Cooperative Adaptive Cruise Control (CACC), which are tolerant to slightly larger latencies but sensitive to jitter and out-of-order delivery. CSC can use a combination of strict priority queuing and credit-based shaping to balance throughput and determinism, with redundant paths to support fail-over.

• Best-Effort & Services Class (BESC): For infotainment, diagnostics, OTA, and telemetry—high bandwidth but low safety criticality. BESC uses standard Ethernet scheduling with policing to avoid interference with higher classes.

A key contribution is an explicit mapping rule: map every function to a class by first determining its worst-case control computation and actuation delay budget and then allocating network deadline as a fraction (e.g., 30–50%) of total allowable loop latency, leaving the remainder for computation and actuator response. While precise numeric fractions should be tuned per use case and validated empirically, the qualitative guidance follows the control literature that highlights the sensitivity of vehicle lateral and longitudinal controllers to network delays (Cao et al., 2019; 2021; 2022).

Function classification and hardware redundancy mapping: We introduce a graded redundancy matrix linking ASIL level, function criticality, and recommended redundancy:

• ASIL D / Safety-critical, fail-operational: Dual-core lockstep with independent comparators and cross-monitoring (Abdul Salam Abdul Karim, 2023). Lockstep is recommended for controllers responsible for emergency braking, core vehicle stability, and other functions that must continue operation post-fault or must detect and silence faults within a deterministic timeframe.

• ASIL B/C / High reliability but not fully fail-operational: Dual independent cores with majority voting or selective lockstep depending on cost constraints; hot-standby replication for some functions where rapid takeover is acceptable.

• ASIL A / Non-critical: Single-core with watchdog and software-based redundancy.

We emphasize that lockstep is not universally optimal—the approach increases cost, power, and complexity and should be selectively applied where the failure modes justify it. The rule of thumb derived is to apply lockstep to functions where transient silence or incorrect actuation within a single control cycle could produce catastrophic outcomes, while using less costly redundancy for functions where delayed recovery is tolerable (Abdul Salam Abdul Karim, 2023; Bandur et al., 2021).

Gateway and legacy integration approach: Legacy buses (CAN, LIN, FlexRay) will persist during migration periods. Gateways must therefore be synthesized automatically from high-level models to minimize human error in message packing and timing (Sander et al., 2011). Gateways should be modeled as TSN-aware services with bounded buffering and deterministic forwarding rules; any translation should account for compounded delays introduced by frame packing on low-bandwidth buses as previously discussed in CANFD frame packing literature (Bordoloi & Samii, RTSS). We recommend that gateways expose health and timing telemetry as services in the SOA layer to enable dynamic adaptation (e.g., when CAN bus load increases, the TSN fabric might prioritize critical control messages through alternate paths).

Verification and validation roadmap: For any proposed configuration, we prescribe a staged validation plan: model-in-the-loop (MiL) to check timing budgets using tools such as RTaW-Pegase and TCN timeanalysis for scheduling analysis (RTaW-Pegase, 2022; TCN timeanalysis, 2022); hardware-in-the-loop (HiL) to validate real latencies, jitter, and failover behavior; and vehicle-in-the-loop (ViL) or fleet pilot to validate end-to-end safety and user experience.

TSN scheduling must be validated both statically (schedule feasibility) and dynamically (reconfiguration under fault or topology change), and the SDN management plane must be tested for secure reconfiguration without violating safety deadlines (Chahed & Kassler, 2021; Hackel et al., 2022).

Discussion

The integrated blueprint implies multiple theoretical and practical implications, raises counter-arguments that must be addressed, and suggests a prioritized research and industrialization pathway.

Balancing determinism and flexibility: TSN provides mechanisms to enforce deterministic behavior but imposes rigidity on scheduling. A central tension is reconciling the hard scheduling needed for CDC with the dynamic reconfiguration favored by SOA and software-defined management. Chahed & Kassler (2021) and Hackel et al. (2022) noted the role of SDN to program TSN fabric; our elaboration argues that a hybrid approach is necessary: static schedules for ultra-critical flows and controlled, policy-driven reconfiguration windows for less critical flows. This hybridization reduces the risk of schedule fragmentation while enabling flexibility for non-critical services. A potential counter-argument is that static schedules increase fragility under evolving service demands; we respond that service abstraction at the SOA layer combined with capacity reservation for BESC traffic can mitigate this by encapsulating change within pre-allocated windows rather than reshaping hard schedules frequently.

The cost-safety tradeoff of lockstep: Dual-core lockstep ensures deterministic fault detection and is compelling for ASIL D controllers (Abdul Salam Abdul Karim, 2023). However, lockstep increases silicon area, power consumption, and heat dissipation—important concerns for zonal controllers located in thermal-sensitive vehicle zones (Schäfer & Denkelmann, 2018). We propose selective lockstep application and hybrid schemes like lockstep for core safety tasks combined with asymmetric cores for non-safety workloads to balance safety and thermal-power constraints. A more contentious alternative is software redundancy and cross-monitoring across distributed ECUs, but this increases network dependency and may not satisfy fail-operational constraints.

Latency budgeting and control stability: The control-oriented literature repeatedly shows that many vehicle control functions are highly sensitive to compounded network and computation delays (Cao et al., 2019; 2021; 2022; 2023). The mapping rule we propose—allocating a portion of the control loop latency budget to the network—has direct implications for where functions are placed (zone vs. central). For controls with sub-millisecond deadlines, zonal placement is often mandatory to avoid unacceptable network traversal and gateway conversions. Conversely, perception-heavy functions (sensor fusion, inference) can be centralized where higher latency is tolerable and compute consolidation yields benefits. Critics might claim that centralization yields better utilization and simpler software stacks (Bandur et al., 2021); we counter that such benefits only hold when the network can provide deterministic latency guarantees that preserve control stability—hence the emphasis on TSN and careful deadline decomposition.

SOA and AUTOSAR Adaptive interplay: The integration of OPC UA service orientation with AUTOSAR Adaptive runtimes provides a promising path to unify discoverability and encapsulate QoS metadata (Arestova et al., 2021; Villanueva et al., 2021). However, the richer protocol stacks of OPC UA and Adaptive introduce extra processing overhead and timing variability. To manage this, the architecture must treat SOA as an overlay: service discovery and metadata negotiation occur at slower timescales, while actual critical control data follows pre-allocated TSN pathways with thin virtualization layers. This separation reduces the runtime jitter introduced by complex middleware. It also suggests revisiting AUTOSAR Adaptive implementation choices to allow a lightweight runtime path for critical services.

Security as a first-class constraint: Hackel et al. (2022) emphasize secure TSN for vehicles; security mechanisms (authentication, encryption, secure key management) introduce latency and processing overheads that interact

with strict timing budgets. We recommend hardware-accelerated crypto modules in zonal controllers, group key management that avoids per-frame public-key operations in fast paths, and careful placement of security gateways such that critical control flows bypass non-essential cryptographic processing while still ensuring integrity and authenticity through lighter mechanisms (e.g., MACs + sequence numbers) validated by secure enclaves. A research gap remains in quantifying the exact latency/throughput tradeoffs of diverse security schemes within TSN contexts.

Gateway synthesis and automatic optimization: Sander et al. (2011) demonstrated that model-based automatic gateway generation reduces manual configuration errors. Building on this, we argue for toolchains that accept high-level functional descriptions, associated safety levels, and timing budgets, and then synthesize both TSN schedules and gateway message packing/priority mappings automatically. This would accelerate architecture iteration and facilitate repeatable verification. However, automatic synthesis raises its own verification burden: the synthesis tools must themselves be certified—or at least demonstrably trustworthy—if they are used to produce code or deployment artifacts for safety-critical functions.

Limitations and uncertainties: The article's primary limitation is its conceptual nature—while the synthesis draws heavily from empirical studies in the literature, it lacks new experimental data. The mapping rules and budget allocations offered are therefore prescriptive rather than empirically validated across diverse hardware platforms. Another limitation is temporal: the references reflect research up to recent years, but industrial practice and silicon availability evolve rapidly; for instance, new SoC families with built-in TSN accelerators could alter the cost/performance calculus (Vitesco Technologies; Robert Bosch GmbH descriptions). Finally, while control literature informs latency sensitivity, modeling real world uncertainty (packet loss bursts, thermal throttling) requires system-level emulation and fleet trials that were beyond the scope of this paper.

Future scope and prioritized research agenda: We propose a staged research roadmap:

1. Toolchain development: Create synthesis and verification toolchains that accept high-level functional descriptions and output TSN schedules, gateway configurations, and redundancy layouts; validate tool correctness under formal methods approaches (Sander et al., 2011).
2. Experimental validation: Use RTaW-Pegase and TCN timeanalysis for static scheduling feasibility and extend with HiL and vehicle trials to measure real performance under failure injection scenarios (RTaW-Pegase, 2022; TCN timeanalysis, 2022).
3. Security/Latency tradeoff quantification: Measure latency overheads of various crypto primitives and key management schemes on representative zonal SoCs, and define hardware acceleration requirements (Hackel et al., 2022).
4. Thermal and power optimization: Study power/thermal envelopes for lockstep zonal controllers and develop hybrid redundancy schemes that preserve safety while respecting thermal constraints (Schäfer & Denkelmann, 2018)
5. Standardization and interoperability: Contribute empirical findings to AUTOSAR and TSN standardization efforts to reconcile SOA middleware overheads with deterministic TSN needs (Arestova et al., 2021; Villanueva et al., 2021).

conclusion

This article synthesizes extensive literature to propose a coherent, practical, and theoretically grounded approach for designing resilient zonal E/E architectures that integrate TSN, SOA, and fault-tolerant hardware strategies. The central contributions are: (1) a layered architecture model that aligns zonal hardware, deterministic TSN fabrics, and service abstraction layers; (2) prescriptive co-design rules mapping function criticality to TSN classes and

redundancy patterns; (3) a gateway synthesis and verification roadmap to manage legacy bus integration; and (4) an articulated research agenda to operationalize and empirically validate the proposed blueprint. The recommendations emphasize selective use of lockstep processors for highest-criticality functions, hybrid static/dynamic TSN scheduling to preserve both determinism and flexibility, and model-based toolchains for automatic gateway and schedule synthesis. While further empirical work—spanning MiL, HiL, and pilot fleet deployments—is necessary, the rules and architectural patterns presented here provide a practicable pathway for OEMs and suppliers seeking to implement safe, deterministic, and scalable E/E architectures in the era of electrification and automated driving.

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