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Research Article

Factory Calibration and Active Regulation of Laser Output in Electronic Control Devices

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Firmware Architecture, Calibration, and Fault Detection in ECD Laser Modules

Abstract

This paper presents the design and firmware implementation of a closed-loop laser power regulation system for electronic control devices (ECDs). A dual pulse-width modulation (PWM) scheme is proposed to achieve precise, temperature-independent control of laser output across Class I, II, and III power levels. A structured factory calibration procedure is described, wherein ADC feedback voltages and corresponding duty cycles are stored in CRC-protected non-volatile memory for each power level. The regulation algorithm is analyzed in detail, including its closed-loop feedback mechanism, fault detection thresholds, and fail-safe shutdown behavior. Additionally, this work examines laser diode efficiency variability encountered during manufacturing—specifically issues arising from PCB routing noise affecting ADC reference accuracy—and presents firmware-based mitigation strategies and pre-screening protocols to address these failure modes. The results demonstrate a robust, multi-layered safety architecture suitable for laser modules in regulated ECD applications.

Keywords: LASER firmware, PWM control, ADC feedback, calibration, electronic control devices, laser diode, power regulation, fault detection, safety firmware.

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1. INTRODUCTION

Electronic control devices (ECDs) employ actively controlled laser diode modules to provide precise targeting assistance. These modules must conform to strict international standards governing optical output power across a range of environmental conditions, including elevated temperature, power supply variation, and component aging. Ensuring regulatory compliance demands a firmware architecture that combines accurate closed-loop power regulation with robust fault detection and fail-safe behavior [1].

Laser power regulation in ECDs is non-trivial due to the inherent temperature dependence of laser diode efficiency, component-level variability across manufacturing batches, and the requirement to support multiple output power classes (Class I, II, and III) within a single hardware platform. These challenges necessitate a calibration-driven approach in which device-specific parameters are measured and stored during manufacture, enabling the firmware to accurately reproduce target output levels under varying field conditions.

This paper investigates the laser feedback control architecture, calibration methodology, closed-loop regulation behavior, fault detection strategy, and mitigation of known hardware anomalies in ECD laser modules. The work draws upon firmware documentation and experimental observations, providing a comprehensive technical reference for laser module development [1][2].

2. ARCHITECTURE OGY

The ECD laser module operates as a subordinate device within the weapon system, activating laser diodes only upon explicit command from a parent handle controller. This master-slave partitioning provides an important safety boundary: the laser module cannot autonomously energize any diode, limiting the impact of firmware faults or communication errors on optical output behavior [1].

The overall system architecture, illustrated in Fig. 1, comprises four principal subsystems: the handle controller, the laser module CPU, the PWM driver stage, and the laser diode array. A feedback path from an optical power monitor returns an ADC-sampled voltage proportional to laser output power. Non-volatile flash memory stores factory-calibrated reference values and a CRC-protected product configuration record.

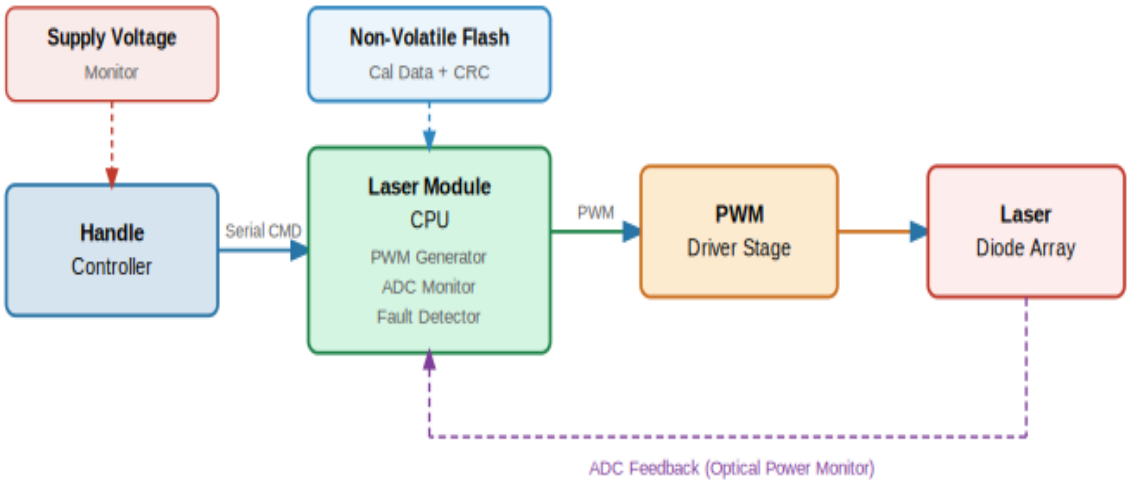


Fig. 1. ECD Laser Module System Architecture

The handle controller additionally monitors the regulated supply voltage to the laser module. Detection of an overvoltage condition causes the handle to power-cycle the module entirely, providing a hardware-level safety interlock that is independent of the laser module firmware and immune to firmware faults within that subsystem [2].

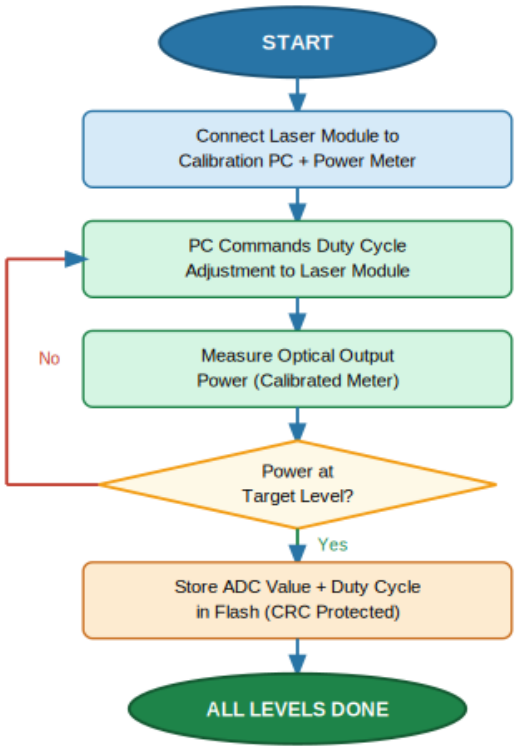


Fig. 2. Factory Calibration Flowchart (per Power Level)

3. DUAL PWM CONTROL ARCHITECTURE

Laser output power is modulated using two PWM channels operating in parallel. The first channel is maintained at a fixed 40% duty cycle across all power classes and operating modes. The second channel is varied dynamically by the regulation loop to achieve the desired optical output power.

A. Rationale for Dual-Channel Design

A single-channel PWM architecture is susceptible to efficiency discontinuities at certain duty cycle thresholds, arising from non-linearities in the laser driver circuit. The dual-channel approach eliminates this problem by ensuring that the combined drive signal never crosses the discontinuity boundary as the dynamic channel traverses its operating range. The fixed channel provides a stable base drive level, while the dynamic channel provides fine-grained power modulation.

The representative waveforms for both PWM channels across the three operating power classes are shown in Fig. 3. The fixed channel waveform remains invariant, while the dynamic channel duty cycle increases progressively from Class I through Class III.

B. Blinking Mode

In blinking mode, the laser is toggled on and off at a defined cadence while the regulation state is preserved. When the laser is re-enabled after a blink-off interval, the firmware reinstates the last known duty cycle, avoiding the latency and transient behavior associated with a full regulation restart. On first-generation ECD platforms, the fixed 40% channel remains energized throughout blinking intervals. Blinking support is present in the second-generation platform firmware but its deployment status in production firmware has not been confirmed.

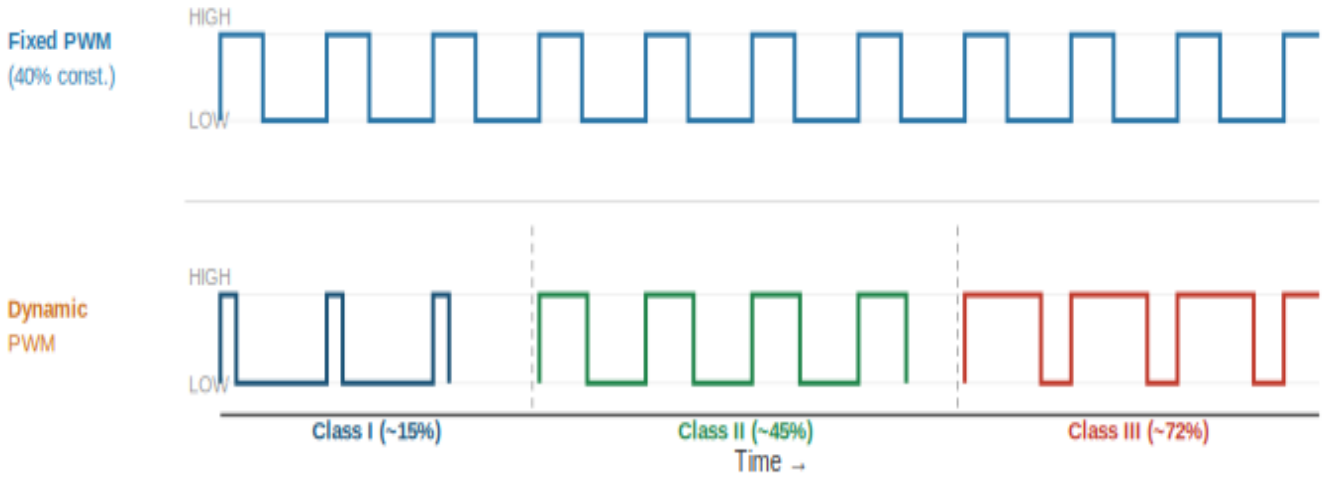


Fig. 3. Dual PWM Channel Waveforms Across Operating Power Classes

4. FACTORY CALIBRATION

Factory calibration is a mandatory manufacturing step performed individually for each laser diode module. Its purpose is to characterize the relationship between PWM duty cycle and optical output power for that specific device, compensating for inter-device variability in diode efficiency, threshold current, and slope efficiency.

A. Calibration Process

Calibration is executed by a PC-hosted application that communicates with the laser module via a serial interface. The PC program issues duty cycle commands to the module and simultaneously samples the optical output power using a traceable, factory-calibrated laser power meter. The duty cycle is incremented iteratively until the measured output converges to each target power level within a specified tolerance. The calibration flowchart is shown in Fig. 2.

B. Calibrated Power Levels

Three power levels are calibrated for each diode:

- Low Power (sub-Class I): A conservative startup level used solely for initial power-up validation of the feedback circuit. This level is set well below Class I regulatory limits.
- Class II: Corresponds to a target optical output of 0.9 mW. This is the standard operational power class for most ECD deployment configurations.
- Class III: Corresponds to a target optical output of 4.0 mW. Used in configurations requiring enhanced targeting visibility.

C. Data Storage and Integrity

Upon completion of calibration, the measured ADC feedback voltage and corresponding duty cycle are stored in non-volatile flash memory as a calibration record. The complete calibration dataset, together with the product class configuration (Class II or Class III), is protected by a 16-bit CRC. Any corruption of the calibration data detected at runtime results in degraded-mode operation, as described in Section VI [1].

D. Calibration Validation

Following data storage, the calibration program executes a validation sequence: the module is power-cycled, and the firmware is allowed to run its normal startup and regulation routine. The program verifies that regulated output power converges to the target level within the specified error margin before the module is accepted. Modules that fail validation are flagged for rework or rejection.

5. CLOSED-LOOP POWER REGULATION

The regulation algorithm implements a discrete-time proportional control loop using ADC feedback from the optical power monitor circuit. The design is intentionally conservative: duty cycle adjustments are limited to single-count increments per cycle to prevent overshoot and to bound the rate of change of optical output power.

A. Startup Validation Sequence

Upon receiving an activation command from the handle controller, the laser module drives the diode at the calibrated low-power duty cycle. A 40 ms stabilization period allows the optical output and photodetector circuit to reach steady state. The firmware then reads the ADC feedback voltage and compares it against the stored low-power calibration reference. Two failure conditions are evaluated: if the feedback voltage is below the expected range, the feedback circuit is considered open or insufficiently responsive, and regulation is disabled while the diode remains at the fixed low-power duty cycle. If the feedback voltage exceeds the expected range, the firmware concludes that the feedback circuit is driving an excessive apparent power level and shuts the diode down entirely.

B. Regulation Loop Operation

If the startup validation passes, closed-loop regulation is enabled. Every 6 ms, the firmware samples the ADC feedback channel and compares the result to the calibrated reference value for the target power class (Class II or III). If the feedback value is below the target, the dynamic PWM duty cycle is incremented by one count. If above the target, it is decremented by one count. This single-count adjustment strategy ensures that the output approaches the target monotonically and that power changes occur gradually, limiting transient excursions.

The regulation state machine is depicted in Fig. 4. The system transitions from IDLE through STARTUP and VALIDATE before entering the REGULATE state. Fault conditions divert the state machine to either a low-power fixed mode or a full shutdown state depending on the nature of the detected anomaly.

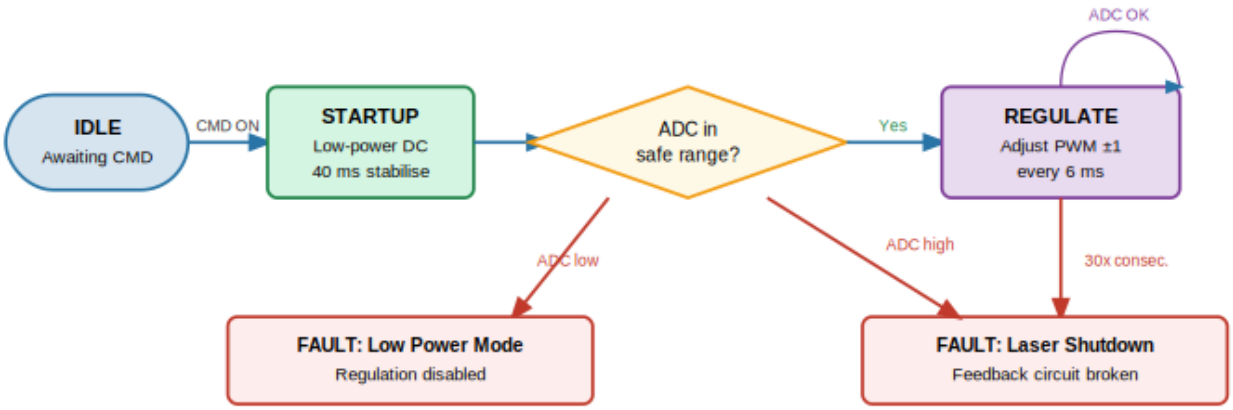


Fig. 4. Laser Regulation State Machine

6. FAULT DETECTION AND SAFETY ARCHITECTURE

The firmware implements a layered fault detection strategy designed to ensure that no single hardware failure can cause the optical output to exceed the calibrated regulatory limit. The following mechanisms operate independently and in concert.

A. Consecutive Step Threshold

The regulation loop maintains a counter of consecutive duty cycle increases and a separate counter of consecutive decreases. If either counter reaches a threshold of 30 consecutive steps, the firmware concludes that the feedback circuit is not responding correctly to duty cycle changes—indicative of a failed photodetector, broken feedback trace, or failed driver component. Upon triggering the increase threshold, the firmware disables regulation and holds the duty cycle at the calibrated low-power level. Upon triggering the decrease threshold, the firmware shuts the diode off entirely, as sustained consecutive decreases suggest the circuit is reporting anomalously high power. Either counter is reset to zero whenever a duty cycle change in the opposite direction is commanded.

B. Firmware CRC Validation at Boot

Before the main firmware application is permitted to execute, the bootloader performs a CRC integrity check over the complete firmware image stored in flash. A CRC mismatch disables the laser module entirely. Following firmware validation, the calibration data and product configuration stored in non-volatile memory are independently CRC-checked. Failure of this second check restricts the module to fixed low-power operation with regulation disabled [1].

C. Hardware Supply Voltage Interlock

Independent of all firmware-level checks, the handle controller monitors the regulated power supply to the laser module. If the supply voltage exceeds a safe operating threshold, the handle powers down the laser module entirely. This interlock operates at the hardware level and cannot be bypassed by any firmware condition in the laser module [2].

D. Communication Partitioning

By design, the laser module will not energize any diode without receiving an explicit activation command from the handle. A failure in the inter-subsystem communication bus therefore results in a fail-safe condition: the laser module defaults to the inactive state. No communication failure mode can produce an over-power output scenario.

7. LASER DIODE EFFICIENCY VARIABILITY

A. Manufacturing Variability

Laser diode efficiency—defined as the slope of the optical power versus drive current characteristic—varies between individual devices within a manufacturing batch and across temperature. The factory calibration procedure compensates for inter-device variability by storing device-specific duty cycles rather than assuming a fixed relationship between duty cycle and power. Temperature dependence is addressed implicitly by the closed-loop regulation mechanism: because the feedback voltage is proportional to actual optical output, the duty cycle is adjusted in real time to compensate for efficiency drift without requiring an explicit temperature sensor.

B. Osram Diode PCB Noise Issue

A manufacturing defect was identified in a subset of second-generation ECD units in which routing noise on the printed circuit board introduced DC offsets in the ADC reference voltage (VREF) line. This error shifted all ADC readings by a fixed but device-specific offset, causing the regulation loop to converge to an incorrect power level. The affected units used Osram laser diodes, whose steeper efficiency curve amplified the impact of the ADC error on optical output power relative to other diode types.

C. Firmware Mitigation

The firmware mitigation strategy reads the actual VREF from a dedicated ADC channel at startup and uses this measured value to normalize all subsequent feedback ADC readings. By computing the feedback ratio relative to the measured VREF rather than assuming an ideal reference voltage, the regulation loop correctly compensates for board-level noise without requiring hardware rework or PCB respins.

D. Pre-Screening Protocol

A complementary manufacturing pre-screening protocol was introduced to identify laser diodes whose efficiency characteristics fall outside acceptable bounds prior to module assembly. Diodes are subjected to a standardized drive current sweep, and optical output power is measured at defined operating points. Devices exhibiting efficiency values beyond a defined tolerance window are rejected before integration into the laser module.

8. DISCUSSION

The architecture described in this paper demonstrates that a reliable, multi-class laser regulation system can be implemented in a resource-constrained embedded firmware environment without external temperature sensors or complex control algorithms. The single-count regulation strategy, while slow to converge relative to proportional-integral controllers, provides inherent protection against overshoot and ensures predictable, bounded behavior in all operating conditions.

The 30-step consecutive change threshold for fault detection represents a balance between false-positive rate and detection latency. At a 6 ms regulation interval, a 30-step threshold corresponds to a fault detection latency of approximately 180 ms—acceptable for the targeting application. Future work should investigate adaptive thresholds that can differentiate between slow thermal drift and genuine feedback circuit failures more rapidly.

The VREF compensation approach for addressing PCB noise is an effective short-term mitigation, but the root cause—inadequate analog supply decoupling on the ADC reference line—should be addressed in future PCB revisions to eliminate the firmware dependency entirely.

9. CONCLUSION

This paper has presented a comprehensive account of the laser power regulation firmware architecture for electronic control devices. The dual-PWM control scheme, factory calibration procedure, closed-loop ADC regulation loop, and multi-layered fault detection mechanisms together form a safety architecture that ensures optical output remains within regulatory limits under a wide range of hardware failure modes, environmental conditions, and manufacturing variations. The firmware-based VREF compensation technique and diode pre-screening protocol provide effective mitigation for laser diode efficiency variability. The architecture described here provides a solid foundation for next-generation ECD laser module designs, with identified areas for improvement in fault detection latency and analog circuit robustness.

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